

Xilinx Design Manager

Xilinx Design Manager with Handel-C

>: 1 Introduction

This application note gives information on how to use Design Manager in the context of a Handel-C design. Handel-C generates EDIF netlists which can be turned into bit files which in turn can configure an FPGA.

>: 2 How to use design manager

When a Handel-C project is built to EDIF format, the resulting edif must be place and routed using Xilinx development tools. This is done by starting Design Manager, and choosing 'New Project' from the File menu.

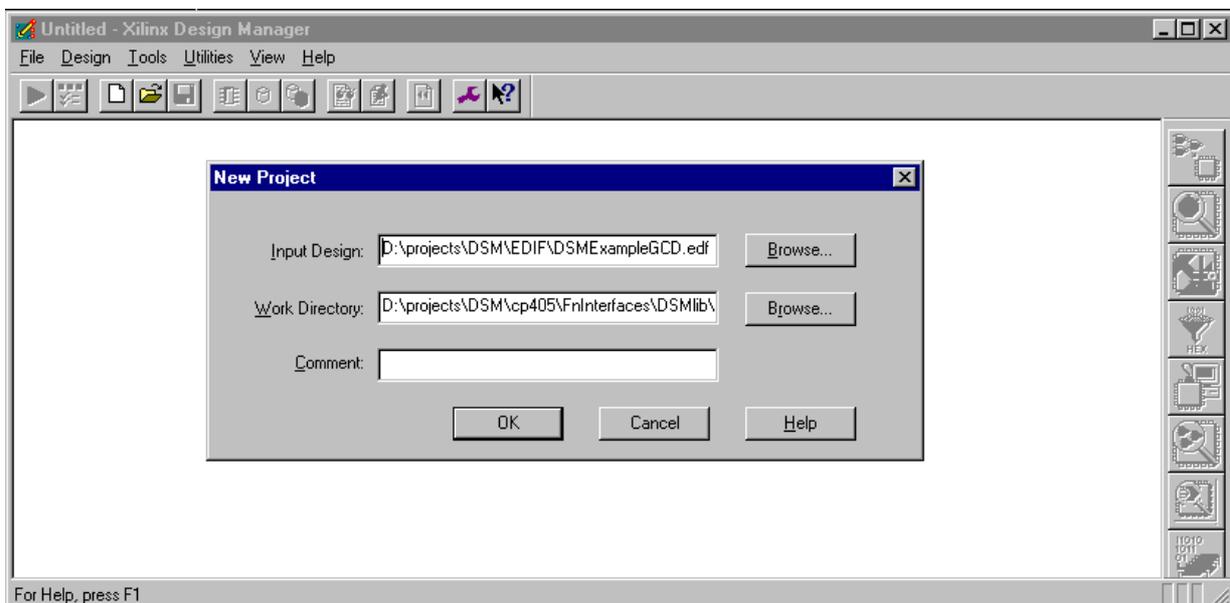


FIGURE 1 - DESIGN MANAGER

The input design is the .edf file with the same name as the project. The working directory can be anywhere that you have write privileges.

When you have created the project (by hitting the OK button) you will be prompted to set up the part settings. Clearly this varies from board to board, and can be read off the top of the FPGA on the target board.

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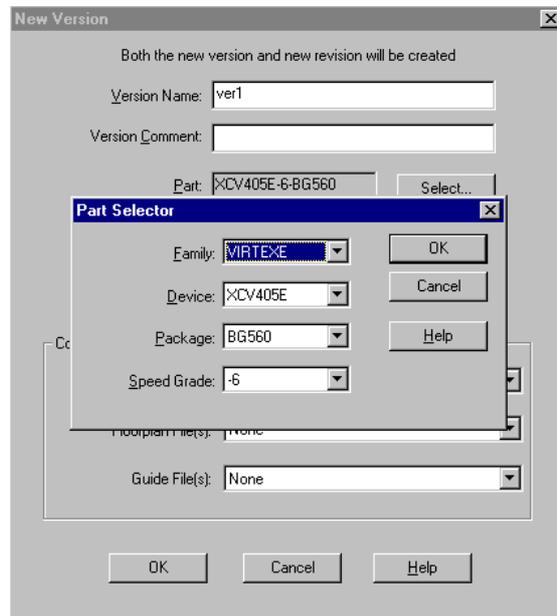


FIGURE 2 - CHIP SETUP

If there is a user constraints file for the project (.ucf) this can be selected here, also guide files (.ncd) and floor plan files (.fnf).

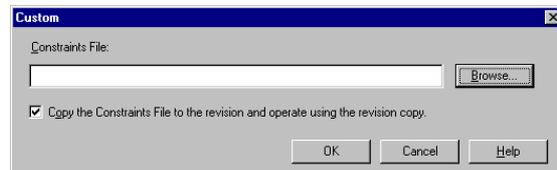


FIGURE 3 - USER CONSTRAINTS FILE

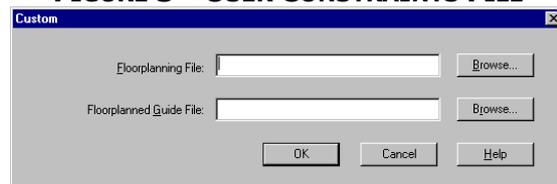


FIGURE 4 - FLOORPLAN FILE



FIGURE 5 - GUIDE FILE

Now you need to select the place and route options. Choose Options from the Design menu. Slide the Place and Route effort level to maximum effort

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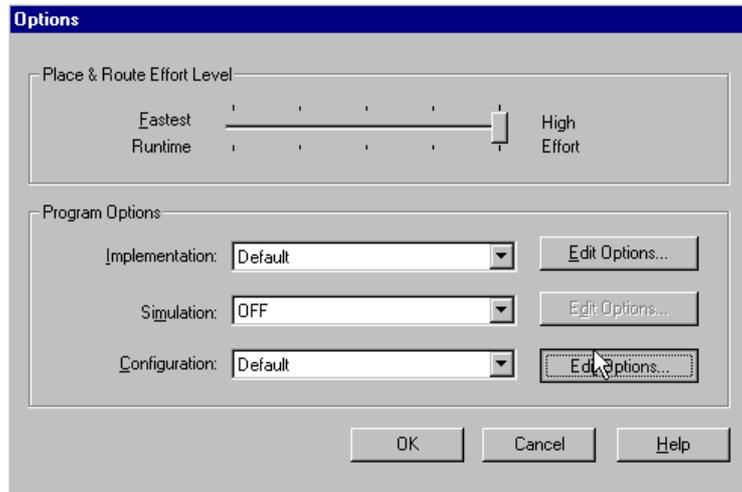


FIGURE 6 - PLACE AND ROUTE AND CONFIGURATION OPTIONS

Now select Implement from the Design menu. When the implementation is complete the .bit file for use with the board will be in the edif directory of the Handel-C project (where the EDIF file was).

>: 3 Advanced Information

Some designs call external netlist blocks e.g. Xilinx coregen blocks, external clock managers, third party code etc. To place and route such a design, the netlist blocks must be in the same directory as the Handel-C .edf file when the project is place and routed.

Some boards/designs require different place and route and configuration options. These are accessible from the screen shown in Figure 6.

If you hit the Implementation button, you can access the flow options. The defaults for these are usually acceptable, and should not be modified unless absolutely required.

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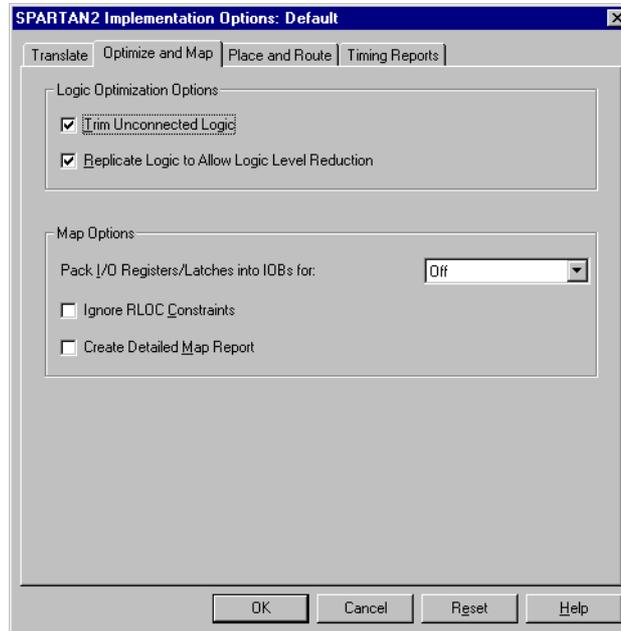


FIGURE 7 - FLOW OPTIONS

If instead you hit the Configuration button, you can set configuration options, allowing the configuration to be changed for different boards. For most boards the defaults are acceptable, and indeed the design may not configure correctly if they are changed. However, for some designs, these have to be changed for the design to work correctly.

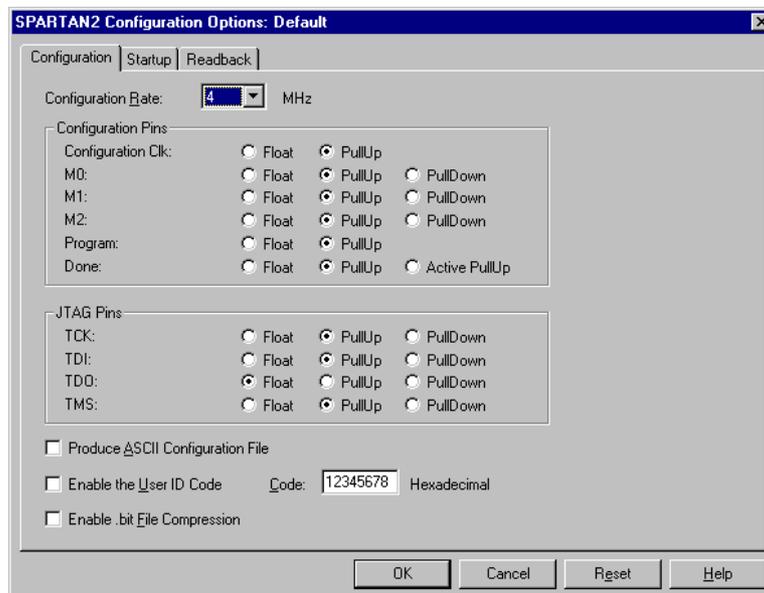


FIGURE 8 - CONFIGURATION OPTIONS

>: Application Note//

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>: 4 Further Information

For information on Celoxica products contact Sales@celoxica.com. Regional office locations are given below.

>: 5 Licensing

This application note, associated documentation, source code and examples are provided for learning and demonstration purposes only.

>: 6 References

[1] DK1 language reference

[2] Xilinx Design Manager Online Help (<http://toolbox.xilinx.com/docsan/xilinx4/>)

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