

# Implementing Complex Algorithms in FPGA's

## Workshop

Argonne Dec02

# >: Implementing Complex Algorithms in FPGAs//

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### >: 1 Requirements

#### Hardware

- The examples use the Celoxica RC100 platform

#### Software

- Acrobat Reader and Microsoft Word to read documentation.
- C/C++ compiler (e.g. Microsoft Visual C++ 6.0 or later)
- Xilinx Place and Route Tools e.g. ISE4
- Celoxica DK1.1 SP1
- Celoxica PDK
- Celoxica RC100 Installation software
- Celoxica RC1000 Installation Software

### >: 2 Tips:

1. To Place and Route your \*.edf netlists:
  - a. Use Xilinx Design Manager: See Application Note 80 "Using Xilinx Design Manager with Handel-C" or
  - b. Use the edifmake batch file found in the Celoxica ADK distribution as follows: Change directory to the location of the netlist e.g the EDIF directory under your DK1 project and type e.g. C:\Progra~1\Celoxica\PDK\Software\Bin\edifmake sevensegment
2. Copy and paste the example code from the word documents --- Cntrl-C (copy) Cntrl-V (paste) --- or use the supplied workspaces and source code files to avoid typing!
3. To Download your design to the RC100 use the RC100 File Transfer Utility. (Launch from the Start Menu). Click Write.... and select bitfile.

### >: 3 Lab #1 - Quick Start DK1, Handel-C and the RC100

Follow Hands On Tutorial HOT -1 RC100 Seven Segment  
Complete at least up to the end of Task 6.

### >: 4 Lab #2 – DK1 New Features

Follow Hands On Tutorial HOT -6 New Features

### >: 5 Lab #3 - PAL API for Platform abstraction

1. Open PAL Examples Workspace from the Start Menu> Celoxica > PDK
2. Select LED as active project
  - Select Simulation Target (Sim)
    - Build Rebuild All
    - Run Simulation (Go)
    - Should see LED 0 flashing on and off
    - Stop simulation
  - Select RC100 Target (RC100)
    - Build Rebuild All
    - Note that the build launches the place and route tools automatically using a "Post build step".
    - Download the resulting bit file to the RC100 using the File Transfer Utility

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3. Try experimenting with some of the other examples in the workspace!
4. For a more detailed insight into the PAL API please refer to the PAL documentation in particular the PAL Tutorial guide (Launch from the Start Menu).

## >: 6 Lab #4 - DSM API for HW-SW comms

1. Open DSM Examples Workspaces (for DK AND VC++) from the Start Menu> Celoxica > PDK
2. Select AddOne as active project in VC++
  - o Target (Debug)
    - Build Rebuild All
    - Run Software Simulation (Go)
    - Enter a value (x) -- Note that software simulation waits for HW sim to start
3. Select AddOne as active project in DK
  - o Target (Sim)
    - Build Rebuild All
    - Run Hardware Simulation (Go)
    - Note return value (x+1)
4. Try experimenting with some of the other examples in the workspace!  
For a more detailed insight into the DSM API please refer to the DSM documentation in particular the DSM Tutorial guide (Launch from the Start Menu).

## >: 7 Further Information

Contact [support@celoxica.com](mailto:support@celoxica.com).  
[www.celoxica.com](http://www.celoxica.com)