The HPC PowerStack: A Community-wide Collaboration Towards an Energy Efficient Software Stack

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WHAT IS THE HPC POWERSTACK INITIATIVE?

- A community-wide collaboration to incorporate power-awareness across various layers of the HPC software ecosystem.
- Since 2016, this collaboration is being supported and driven by a broad spectrum of vendors, labs, and academia that focus on different layers of the HPC stack.

CURRENT LIST OF PARTICIPATING MEMBERS (and growing!)

- **National labs**: LLNL, LANL, Sandia, Argonne, Riken, STFC/Hartree, Cineca, LRZ, Grenoble
- **System Integrators**: Cray, Fujitsu, HPE, ATOS/Bull, IBM
- **Chip Vendors**: x86 (Intel, AMD), ARM, POWER (IBM)
- **Job scheduler / Resource manager vendors**: PBSPro (Altair), ALPS (Cray), Cobalt (Argonne), Flux (LLNL), LSF (IBM)
- **Academia**: TU-Munich, TU-Dresden, UniBo, SDU, Univ of Tokyo, LRZ
- **Facility and Operations**: EEHPC-WG (Energy Efficient HPC Working Group)

CONTRIBUTING TO THE POWERSTACK COLLABORATION

The HPC community is invited to participate in working groups, contribute to the design of the PowerStack, and subscribe to:

- Mailing lists for announcements: powerstack-announce@googlegroups.com
- Slack channel for discussion: https://powerstack.slack.com
- Git repo for open collaboration: https://github.com/powerstack

COLLABORATION CHARTER

(A) Identify key software actors needed in a system power stack: job-schedulers, application-runtime, hardware knobs

(B) Understand the roles and responsibilities of the actors

(C) Reach a consensus on their interoperability

(D) Emphasize on portability (thereby keeping the collaboration vendor-neutral)

(E) Combine existing R&D prototypes and build a community that actively participates in development and engineering efforts.

SNAPSHOT OF RESULTS FROM THE THREE WORKING GROUPS

SYSTEM LEVEL POWER STEERING: WORKING GROUP 2

**R&D goal**: Opportunity Analysis of Power-aware Scheduling in Overprovisioned Resources

**Active Contributors**: Univ of Tokyo/Riken, LLNL, Related Publication: Preprint article - (A)

**Emergent Analysis**: An increase in system-size leads to wasted power that can instead be redirected towards applications for boosting performance.

APPLICATION LEVEL PERFORMANCE AND POWER BALANCING IN POWER CONstrained SYSTEMS: WORKING GROUP 2+3

**R&D goal**: Design and develop community’s first open source application-level power management framework - called GEOPM (https://geopm.github.io), which can co-exist with different layers of the HPC software stack.

**Active Contributors**: Argonne, LLNL, Hartree, LRZ, Cineca, Sandia, IBM, ARM, Marvell, HPE, cray, Intel, TUM, UniBo, U. of Tokyo, U. of Arizona, EU WP

**Related Publication**: Preprint article - (B)

**Emergent Analysis**: 9% to 30% of performance improvement depending on an application design and architecture of power-constrained systems.

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PROJECT ROADMAP AND METHODOLOGY

First community-wide face-to-face seminar • Identify existing state of the art • Solutions at various levels of the stack

Second community-wide face-to-face seminar • Identify interoperability challenges among multiple layers • Biosketches on different engineering approaches • Demand evaluate end-to-end prototypes solutions

PROJECT ROADMAP AND METHODOLOGY

Explore opportunities for standardization • Incorporate PowerStack • Continue discussions and evaluation of solutions

RECENT PUBLISHED LITERATURE

2. The PowerStack Initiative (A Community-driven Effort) - EEHPC-WG Webinar Series, October 2018
6. Power and Performance Optimisation at Exascale - InsideHPC, March 2018
7. Energy efficiency and the software stack - Intel-PPC, December 2017
8. A global survey of HPC center energy and power-aware job scheduling and resource management, November 2017